

Description

The SUPI4-IP is the conversion of the new INTERBUS slave protocol chip SUPI4 in an FPGA. This next generation of the INTERBUS industry standard meets both current and future automation requirements with new and improved system functions. In addition to supporting new system features, it also optimizes interface technology. With the SUPI4, INTERBUS interfaces can be implemented faster, easier, and more cost-efficiently.

The SUPI4 offers the following innovations:

- ▶ 3.3 volt technology
- ▶ Application-specific data signaling rates of up to 16 MBit/s
- ▶ Automatic detection and adjustment of data signaling rate
- ▶ Non-reactive switching of all interfaces
- ▶ Expansion of internal registry structure to up to 64 bytes for data input and up to 64 bytes for data output
- ▶ Parallel and serial microcontroller interfaces
- ▶ Flexible I/O interfaces
- ▶ Easy peripheral diagnostics
- ▶ Configurable performance of digital outputs after a reset
- ▶ Data rate and reset output, as well as internal watchdog for external microcontrollers
- ▶ Configuration through serial EEPROM
- ▶ Simple Profinet integration

The SUPI4-IP includes all of the features of the SUPI4. It provides a connection to Altera's NIOS II; alternatively, other microcontrollers can also be integrated into the system. This allows the combination of the SUPI4, the governing microcontroller, and application-specific logic in one chip.

Features of the SUPI4-IP

- ▶ Compatible with the SUPI4
- ▶ Connection to Altera's NIOS II
- ▶ Supported by SOPC Builder
- ▶ Compatible with the Interbus Master from Phoenix Contact
- ▶ Compatible with the entire Altera product line
- ▶ SUPI4-IP dimensions
 - <6000 LEs and 6k memory bits in the Altera Cyclone II product line
 - <3000 ALUTs and 6k memory bits in the Altera Stratix II product line

Interfaces

The SUPI4-IP has several interfaces. The INTERBUS data interface is responsible for communications with the INTERBUS. The SUPI4's status information can be read on the INTERBUS diagnostic interface. Furthermore, the SUPI4 includes an EEPROM controller, through which an external EEPROM can configure the SUPI4. This configuration can also be manipulated through a serial or parallel microcontroller connected to the multifunction port.

Product Information
Interbus-SUPI4-IP

Licensing Model

▶ *Evaluation Package:*

Complete design with Altera's NIOS II and peripherals for temporary testing in EBV Cyclone Evaluation Board DBC2C20.

▶ *Production Package:*

MAZeT GmbH provides a simple testing program and documentation.

MAZeT Support

System design

Software and driver support

MAZeT's Range of Services

MAZeT GmbH is a company specializing in systems integration of hardware, software, ASIC/FPGA, and optoelectronics. Specific electronic components and systems for medical applications, automation, and industrial testing can be developed according to customer specifications, or they can be mass-produced.

New standards, especially in communications, demand ever-higher requirements, such as "integration," "Internet-capability," and "miniaturization." MAZeT uses the latest technology in order to develop the optimal integration of hardware and software.

Our hardware engineers have extensive expertise in the development of reliable circuitry. We support our customers through the entire process, from articulating their ideas to developing a plan and implementing it. We deliver comprehensive expertise to our customers in the development of innovative circuit designs, the selection of suitable parts, and the consideration of application requirements. Our core competence is the development of field bus interfaces.

Further information is available on our web site at <http://www.MAZeT.de>
or from our sales office!