

All information contained in this Data Sheet is the property of MAZeT. Nothing in this catalog may be reproduced or multiplied in any way, neither electronically nor mechanically, unless the express approval of MAZeT GmbH has been procured. Any company and brand and product names quoted herein are typically subject to trademark, patent or proprietary protection right.

VERSION CHANGES

NO.	ISSUE	APPROVED
1	V1.4	2002-07-09

Data Sheet

MSI 01

Sensor Interface IC

Table of contents

1. FUNCTION	2
1.1. General	2
1.1.1. Features	3
1.1.2. Applications	3
1.1.3. MSI-EB1 Evaluation Board	3
1.2. Analog Components	4
1.2.1. Power Supply	4
1.2.2. Signal Processing	5
1.2.3. Sensor Interfacing Connections	7
1.3. Digital Components	8
1.3.1. Register Block	8
1.3.2. Serial Interface	12
1.3.3. Logic Control Block	14
1.3.4. Signal Declarations	15
2. ELECTRIC PARAMETERS	17
2.1. Absolute Limit Values	17
2.2. Operating Parameters	17
2.3. AC/DC Features	18
3. DESCRIPTION OF MSI 01 PACKAGE	21
3.1. Ordering Specifications	21
PQFP44 Package Dimensions	21
3.3. Pin-Out Assignments	22
4. APPLICATION CIRCUIT	23

MAZeT GmbH Sales
 Göschwitzer Straße 32
 07745 JENA / GERMANY
 Phone: +49 3641 2809-0
 Fax: +49 3641 2809-12
 E-Mail: sales@MAZeT.de
 Url: http://www.MAZeT.de

Approvals

Date

MAZeT GmbH

Compiled: 2001-03-16

Status: valid

Checked: 2002-07-09

Released: 2002-07-09

DOC. NO: DB-99-085e

Page 1 of 23

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

1. Function

1.1. General

The MSI 01 is a highly integrated sensor interface IC capable of processing the signals from up to four differential-output sensors on its input side. It is specifically designed for interfacing with bridge sensors that deliver ratiometric output signals. An input circuit which is configurable in terms of gain, zero-point and resolution amplifies, filters and converts the incoming analog signals into digital ones. They are then made available at a digital interface by a downstream evaluation module.

The MSI 01 offers two possibilities of temperature compensation:

- 1) An on-chip integral temperature measurement that can be used e.g. to compensate the temperature behaviour of connected sensors and that of the MSI 01.
- 2) An external temperature compensation that measures the response of a bridge resistor to temperature changes against a voltage divider (see section. 1.2.3. Sensor Interfacing Connections).

In addition to its integrated on-chip functionality, the MSI 01 notably features a very high signal resolution while maintaining signal stability and consuming little current.

The MSI 01 is designed to evaluate differential sensor signals of the type as delivered by e.g. pressure sensors, hall sensors and sensors working on the principle of a resistance measuring bridge (strain measuring bridges, piezo or magneto-resistive sensors). These sensors are activated by the MSI 01. Per working cycle, current is only supplied to the sensor bridge and only for as long as measurement lasts. Power supply of the bridge circuit can be in current mode or voltage mode.

Equipped with an additional option for recording a '0' input voltage (auto zero) or the voltage of an internal or external calibration divider, the MSI 01 allows balancing to be performed at zero value or full scale value. Since the preamplifier works based on the chopper principle, very small signal amplitudes can be evaluated. The chopper transforms a given input signal into a frequency range such that interferences in the transmission channel will only be caused by the low level of white noise portions. As a consequence, 1/f noise portions prevailing in the low frequency and DC ranges are strongly suppressed.

Because of its small dimensions (PQFP44) and little power consumption (2 mA and 3 uA in stand-by mode resp.), the MSI 01 can be directly mounted at the sensor (e.g. in sensor heads), and sensors which are connected via the MSI 01 can be directly supplied with current and voltage.

Thanks to its integral temperature sensing ability, the MSI 01 can preferentially be employed where sensor characteristics have to be corrected for matching to temperature conditions (e.g. Hall sensors or strain measuring bridges), and further where integrated signal conditioning solutions are required.

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

1.1.1. Features

- Four input channels (multiplex)
- Bridge current or voltage is supplied via the MSI 01 just for as long as the selected sensor bridge takes to finish measurement
- Low power design allows battery-operated mode
- 15-bit resolution
- Charge balancing ADC for excellent noise suppression
- Unipolar and bipolar measurement
- 'Background measurement' mode allows measurement without activation of μC
- Small temperature coefficient due to in-chip and external temperature measurement
- Interrupt is generated on excession of limiting value
- Data output via serial interface
- Built-in pulse counter for use as gas flow meter (gas meter)

1.1.2. Applications

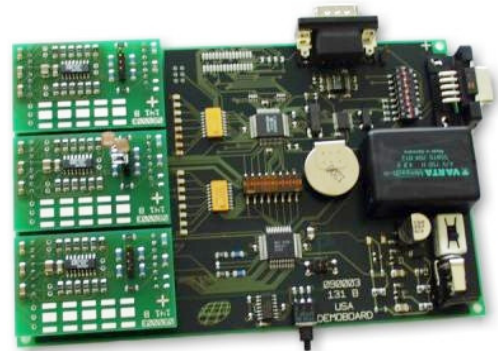
- Battery-supported sensor electronics (pressure, temperature, strain gauge, etc.)
- Data logger for measuring pressure and temperature in gas and water supply nets
- Autonomous gas pressure monitoring devices
- Weather stations
- Gas meters (gas quantity meters)

1.1.3. MSI-EB1 Evaluation Board

The evaluation board provides three plug-in bases for sensor modules to allow individualized connection of those sensors which the user needs to evaluate. The test environment is completed by a Windows-based graphical user screen for fast and easy access to the MCI's functionality.

Features of this user screen include sample configurations of the MSI 01, consecutive measurements with graphical representation of results, access to all MSI 01 configurations (bits).

The graphical user screen ensures easy availability of the whole range of MSI 01 functions and parameters.



Evaluation-Board MSI-EB1

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

1.2. Analog Components

1.2.1. Power Supply

Figure 1 shows a separate MSI 01 power supply diagram.

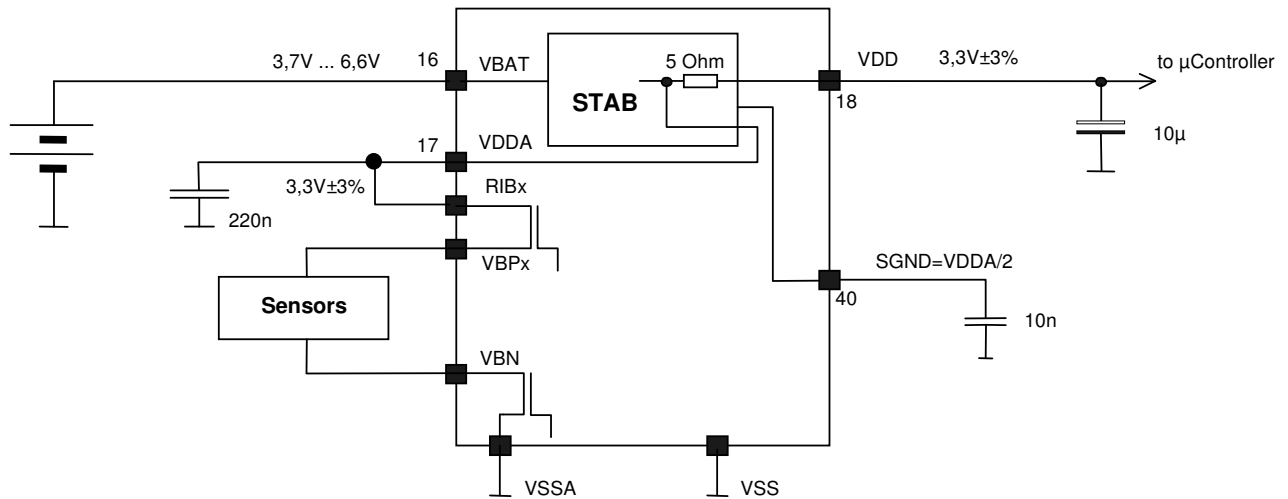


Figure 1: MSI 01 power supply

For MSI 01 operation, a voltage of 6 V is supplied, preferentially from a battery via an on-chip in-phase regulator (STAB). It outputs a stabilized voltage V_{DDA} of about 3.3 V which also powers the bridge sensors. Since the absolute voltage value is subject to relatively broad process tolerances (about $\pm 10\%$), the serial interface is prepared to calibrate to approximately $\pm 3\%$. The regulator has a built-in reset function (PON) to output a static reset signal (high-active), as soon as the operating voltage drops below the power-fail threshold. On excession of this power-on threshold, the reset signal will switch off with a certain time delay.

At the same time, the V_{DDA} supply voltage is also used as reference voltage for the ADC, which ensures ratiometric measurement of the bridge signals. A derivative of the V_{DDA} supply voltage is the V_{DD} voltage which is intended to power an external controller and further system components.

To reduce retro-interference effects from the controller's operating voltage, a resistor of about 5 ohms isolates the V_{DD} voltage from V_{DDA} (regulator output voltage).

With the MSI 01 in power-down mode, all analog circuitry parts, including also the bridge supply components, are turned off. The in-phase regulator will continue to operate in a current saving stand-by mode (diminished regulation dynamics) so as to preserve the data contents of all digital registers, keep the interface in operating condition and maintain power supply of external components.

The reset circuit will also remain active. Because this leads to a change in the regulator's working point, the regulator output voltage may in stand-by mode insignificantly differ from that in normal operating mode ($\Delta V_{DD} < 100\text{mV}$).

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

1.2.2. Signal Processing

A block diagram of the MSI 01 is contained in Figure 2. A required external or internal signal is selected by an input multiplexer (MUX) to be connected to the input of the measuring channel. Supported measuring modes are:

- Differential measurement $IP_x - IN_x$
- Differential measurement $(IP_x + IN_x)/2 - IC_x$ (only for inputs 1 and 2)
- Measurement of on-chip temperature sensor voltage
- Measurement of battery voltage via internal voltage divider
- Auto zero measurement (both inputs of measuring channel internally connected to AGND)
- Measurement of different pick-offs of a symmetric internal calibration divider (ratiometric)

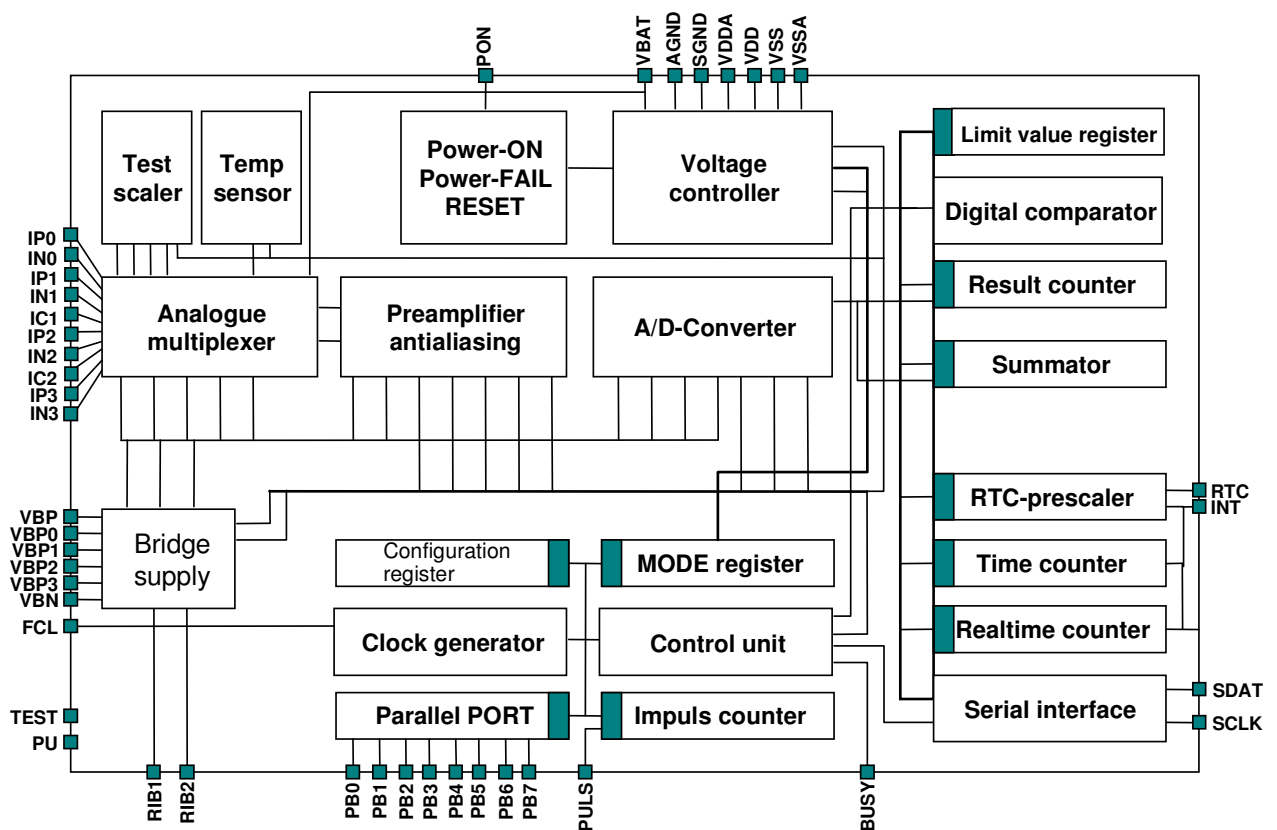


Figure 2: Block diagram of MSI 01

The measuring channel consists of a low-noise preamplifier (CVV) with four selectable gains, one filter amplifier (FV) for signal band limitation and an AD converter (ADC) with four selectable zero-point levels and four selectable resolutions. Configuration of the measuring channel (source, sensitivity, zero-point, resolution) is performed with the help of an interface command before or on starting of measurement.

Battery voltage measurement is restricted to a V_{DDA} range of +0.1 V to approximately 7.2 V, because adequate measuring accuracy is not guaranteed with smaller voltages. Battery voltage measurement must be calibrated as the supply voltage which serves for reference voltage is subject to relatively strong exemplary variations.

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

To measure the chip temperature, an on-chip temperature sensor (TEMP) is provided. Temperature measurement must be calibrated, because notably the sensor offset is subject to major variations. Since V_{DDA} serves as reference voltage, the V_{BAT} dependence (via line regulation!) must be included in the procedure of calibration.

By connecting a capacitor to the FCL pin, the on-chip clock generator (CLKGEN, 256 kHz nominal rate) can be made to work with a lower frequency or the generator clock can be overwritten by an external CMOS clock that is supplied to this pin. In clock-overwrite mode, the external clock needs to be stopped during power-down in low state, in order to prevent unwanted current flows. When working in on-chip frequency mode, you should make sure that there is no parasitic capacity applied at pin CLKGEN (do not connect this pin!)

The series resistor works like a chopper, in order to keep noise portions and drift effects at a minimum. The filter amplifier is intended to re-amplify, symmetrize and limit the signal to a band smaller than 50 kHz (antialiasing).

Designed in switched capacitor technology, the ADC uses the charge balancing method. The converter's integrational behaviour causes a limitation in the bandwidth of noise portions, depending on integration time. For 15 bit-resolution and 256 kHz clock frequency, the integration time is 128 ms. For 13-, 11- and 9-bit resolution, integration time drops by a factor of 0.25 with each transition to the next smaller bit length to correspond to 2 ms for 9-bit resolution. A conversion process consists of a filter settling time (8 ms, 4 ms, 2 ms, 1 ms depending on the selected resolution) and the integration time. Conversion is preceded by a setup time TSET for a selected bridge. It can be selected in a stepping as follows: 2 ms, 8 ms, 32 ms,

128 ms. The ADC's zero-point can also be shifted in such a way that the corresponding input voltage span (span0 ... 3) is broken down from $-1/16 \dots 15/16$ (unipolar) to $-1/8 \dots 7/8$, $-1/4 \dots 3/4$ to $-1/2 \dots 1/2$ (bipolar) (zero... 3). A marge of approximately 3% needs to be deducted from these theoretical ranges on both ends in order to account for a certain offset spread across the entire measuring channel (already accounted for in specified Span values).

In analog testing mode, internal reference voltages are switched on instead of the various external and internal sources. These reference voltages provide the ratiometric input signals for each span. In test mode, the AZ bit causes a pole reversal of the internal reference voltage. This also allows the bipolar measuring ranges to be included in testing.

VERSION		
NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

1.2.3. Sensor Interfacing Connections

A sensor connection sample diagram is shown in Figure 3 with MSI 01 input meanings as follows:

- I0, VBP0: External calibration divider
- I1, VBP1: Bridge in voltage mode with series resistor (to allow temperature measurement via bridge temperature coefficient as described for current mode), at IC1 reference potential for T-measurement
- I2, VBP2: Bridge in current mode, at IC2 reference potential for T-measurement
- I3, VBP3: Bridge in voltage mode with two series resistors

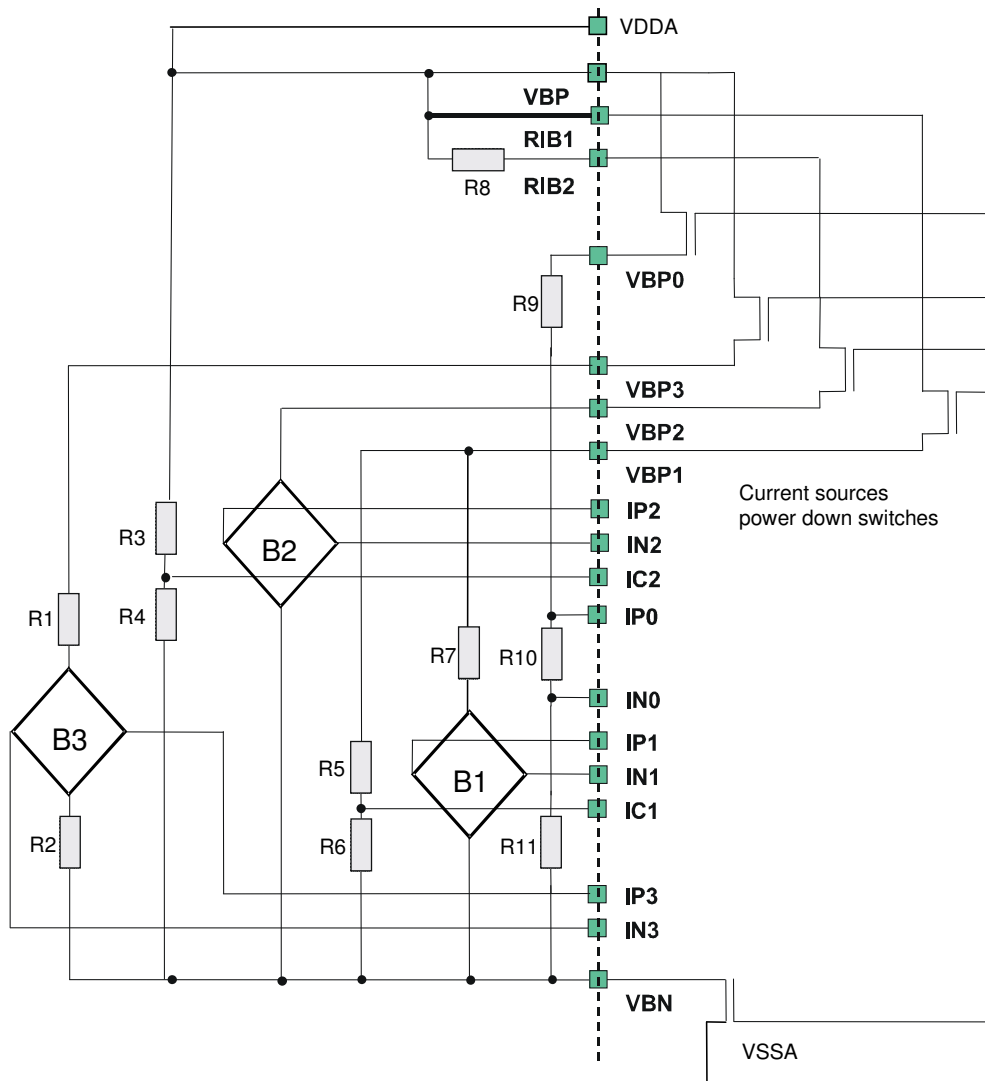


Figure 3: Connection diagram to power measurement bridges in voltage mode and current mode

Sensors which are not designed as bridge circuits can also be connected. With non-ratiometric signals, one should however consider that the operating voltage and notably its temperature coefficient will be reflected in the conversion result. It should further be guaranteed that the common-mode level is within specified limits.

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

All inputs (I0 ... I3) are rated for differential measurement (IPx: positive input, INx: negative input). For a typical application scenario of four bridge sensors, four switched supply pins (VBP0 ... VBP3) are provided. These are activated each time when a channel is selected for measurement. This is done in order to keep the mean operating current as small as possible.

Two of the external bridge sensors (VBP1, VBP2) can be supplied in current or voltage mode, all others in voltage mode only. For current supply mode, a current source is available (BSUPPLY) to provide a constant current of VDDA from (source / STAB) via pins VBP1 or VBP2. Distinction between current and voltage supply mode is achieved by different RIBx pin connections: A short circuit with VBP results in voltage supply mode (RIBx connected with VBP). Using an external resistor for the current sources is a necessary precondition for a small temperature coefficient. Simultaneously, it adds flexibility to the use of the various bridge resistors ("coarse balancing"). In order to minimize the influence of internal drift effects, the current source's regulating amplifier is choppered. Additionally, supply currents can be matched to the specified bridge resistor tolerances in eight steps ("fine balancing", configuration via interface command), and are proportional to the supply voltage VDDA so ratiometric measurement will also be guaranteed in current supply mode.

Resistance RIBx will be calculated by following equation:

$$R_{IB} = (V_{DDA} / I_{out}) * 0.05 \quad I_{out} - \text{bridge current}$$

For temperature measurement involving the temperature coefficient of bridge resistors, which typically lies between 2000 ppm/K and 4000 ppm/K for piezoresistive bridges, the common-mode voltage of the bridge's diagonal (internal averaging of inputs IP1/2 and IN1/2) can be measured against an external voltage divider (inputs IC1, IC2). As a compulsory precondition therefore, current supply mode must be chosen with signal voltages typically in the range of approximately 2 to 4 mV/K (3 ... 4 kΩ bridge resistance, about 0.75mA bridge current).

1.3. Digital Components

The digital part of the MSI 01 consists of a register block, a serial two-wire interface (TWI) and a logic control block.

1.3.1. Register Block

The TWI allows reading and writing of the digital part registers. These are intended for configuration, control and storage of measured values. In normal operating mode, only certain read and write operations make sense. Each register can be accessed via its own register address. The following table lists all registers and the significance of respective register bits in the selected order of addresses.

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

Name	Address	Length	Reset value	Meaning
KONFIG	0x0000	2 bytes	0000	Configuration register
ERGEB	0x0001	2 bytes	0000	Result register
ERGSUM	0x0002	3 bytes	000000	Result register (cumulating)
RTCSET	0x0003	1 byte	00	RTC counter (preloadable)
GRENZ	0x0004	3 bytes	000000	Limit value register
IMPZAHL	0x0005	3 bytes	000000	Pulse counter
ZEITZA	0x0006	2 bytes	0000	Time counter
PORT	0x0007	1 byte	00	Port register
MODE	0x0008	1 byte	00	IC configuration register
RTCVT	0x0009	2 bytes	0000	Register for RTC prevision factor

1.3.1.1. Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
K[2:0]			AZ	E[1:0]		O[1:0]		A[1:0]		I[2:0]			SW	TM	SR

Bit(s)	Meaning	Values	Configuration
K[2:0]	Measuring input selection	0	Channel 0, bridge 0, (IP0, IN0)
		1	Channel 1, bridge 1, (IP1, IN1)
		2	Channel 2, bridge 1, (IP1/N1, IC1)
		3	Channel 3, bridge 2, (IP2, IN2)
		4	Channel 4, bridge 2, (IP2/N2, IC2)
		5	Channel 5, bridge 3, (IP3, IN3)
		6	Channel 6, chip temperature
		7	Channel 7, battery voltage
AZ	AutoZero	0	Measures selected channel
		1	with TM = 0: measures zero-point with TM = 1: reverses calibration divider poles
E[1:0]	Span selection	0-3	Span 0-3, 0 = 300 mV; 3 = 10 mV
O[1:0]	Zero-point (Offset)	0-3	Zero 0 to Zero 3
A[1:0]	Resolution/conversion time	0	9 bits / 3 ms + T _{SET}
		1	11 bits / 10 ms + T _{SET}
		2	13 bits / 36 ms + T _{SET}
		3	15 bits / 136 ms + T _{SET}
I[2:0]	Bridge current setting	0-7	Step 0 to Step 7
SW	Conversion start	0	Only configuration
		1	Starts a foreground conversion
TM	Analog test mode	0	Normal switching function
		1	Test mode channels with K[2:0], AZ selected
SR	Soft reset	0	
		1	Aborts a running measurement

This register is designed for configuration and triggering of measuring processes. It can also be used to abort a running measurement. With bit SW set to '1', a measurement will be triggered on detection of the interface stop condition. On completion of measurement, bit SW will be reset to '0'. With SW=0, the converter can be reconfigured. With SR=1 (bit is not stored), a running measurement can be aborted and a defined state for starting a new measurement can be restored.

Besides, some test functionalities are also handled via this register.

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

1.3.1.2. Result Counter

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GF	ERG[14:0]														

Stores the result of a single measurement. A measured result (ERG) may contain any value between 0 and 32767 ($2^{15}-1$). The MSB of a measured result is assigned to bit 14 independently of the selected resolution (left-adjusted results). All bits that are unused in a lower resolution mode are connected to level '0'. The counter is reset on each start of a new measurement.

1.3.1.3. Results Sum Counter

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OF	ERGSUM[22:0]																						

Sums up the result of single background measurements and stores it on completion of measurement. If an overflow occurs during measurement ($Z_{out}=(2^A - 1)$), the overflow bit OF will be set. The counter is reset on writing of RTCSET.

1.3.1.4. Real Time Clock Counter

7	6	5	4	3	2	1	0
RTCSET[7:0]							

Allows selection of a desired number of background measurements. After each background measurement, the counter is decremented. This limits the maximum possible number of background measurements to 2^8 (256). Data writing into this counter is the starting condition for so-called background measurement. Once the counter reaches '0' value, background measurements will stop. Subsequently arriving RTCINT pulses will not have any influence on the counter reading. The counter is reset as part of a soft reset.

1.3.1.5. Limit Value Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OBGRZ[10:0]												B ₁₂	B ₁₁	UNGRZ[10:0]									

Defines the MSB of the upper limit (OBGRZ) and that of the lower limit (UNGRZ) of a measured value to be converted. If there is positive excession of the upper or negative excession of the lower limiting value, a running background measurement will be terminated early (RTC counter unequal zero) and the MSI 01 switch to power-down mode. Both limiting values OBGRZ and UNGRZ are completed to 16 bits so each of them may take on values between 0 and $2^{16}-1$ (65535) in steps of 32. If UNGRZ=0x000 and OBGRZ=0xFFE is written into this register, no limit values will be monitored and background measurement not be terminated early. Bits 11 and 12 are for optional changes in the functionality of the analog part. Their default value is 0.

When results are out of range bit 15 (GF) of result counter will be set to ,1'.

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

1.3.1.6. Pulse Counter

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMPZAHL[23:0]																							

Counts the pulses arriving at the PULSE input. Is only reset on "Power On" and can thus be used for differential measurement. Allows no writing.

1.3.1.7. Time Counter

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZEIT[9:0]										0	0	0	0	0	0

Counts the predivided RTC pulses (RTCINT). Is only reset on Power-On and can thus be used for differential measurement. Allows no writing.

1.3.1.8. Port Configuration Register

7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

The PORT register supports configuration of the freely programmable eight-bit digital port. The signal levels which are declared in this register will be available at its outputs PB[7:0].

1.3.1.9. Mode Register

7	6	5	4	3	2	1	0
INT[1:0]		POL	FCH	AV[1:0]		ST[1:0]	

Bit	Meaning	Value	Configuration
INT[1:0]		0	No interrupt (default level as per POL bit)
		1	END interrupt
		2	RTCINT interrupt
		3	END/RTCINT interrupt
POL	Polarity of INT signal	0	Low-active (default = high)
		1	High-active (default = low)
FCH	Chopper frequency	0	4 kHz (default)
		1	8 KHz
AV[1:0]	VDD balancing (in 5% steps)	0-3	4 steps for voltage balancing highest voltage at 0
ST[1:0]	System settling time	0-3	Additional measurement system settling time of 2, 8, 32 or 128 ms

This register is intended for MSI 01 configuration. It is only reset on Power-On.

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

1.3.1.10. RTC Predivider Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VT[15:0]															

Divides the pulses that arrive at input RTC. By writing into this register, one may set a desired division factor. A content of FF represents the greatest possible division factor of 32767:1. A content of 00 will block RTC pulses. The predivider register is only reset on Power-On. The actual predivider part is reset on writing into the predivider register. Following division, the RTC pulses (RTCINT) trigger background measurements and are available at output INT (if MODE register was appropriately set) for interrupt control.

1.3.2. Serial Interface

1.3.2.1. Features

Equipped with a bi-directional pin (SDAT) and an input pin (SCLK), the serial interface represents a two-wire communication port. The SDAT pin has an open-drain output stage. By connecting a variety of devices to these two pins a serial bus can be organized. As long as the bus is not used, the two pin lines are kept on high level by external pull-up resistors. As a basic rule for this serial bus, a low is always the dominant line signal which will overwrite a high in every case, whereas a low can never be overwritten by a high. The data transfer rate is up to 100 kbit/s in standard mode and up to 400 kbit/s in fast mode.

1.3.2.2. Principle of Serial Bus Data Transfer

The data which is clocked with the SCLK line is transferred on the SDAT line by the serial bus. Data are only regarded as valid as long as the clock on SCLK is in HIGH state. Bus data transfer is byte-wise organized, beginning with the MSB, i.e. each byte on SDAT is eight bits long. There is no limitation in the number of transferable bytes. When the bus is inactive, SDTA and SCLK are high. A data transfer is enabled on a high-low level transition on SDAT, with SCLK remaining at high level (starting condition). After occurrence of a starting condition, the seven-bit long device address (DevID) is transferred. This is followed by bit R/W which sets a data transfer direction. The ninth bit then contains the expected acknowledge signal from the slave to the master. Finally, the data is sent in packages of eight bits and acknowledged with a ninth bit. A data transfer terminates on arrival of a stop condition which is achieved with a low-high transition on the SDAT line. Again the CLK line carries high level when this control signal is present. Figure 2 contains a schematical data transfer diagram. The serial interface provides no algorithms to test or remove transfer errors.

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

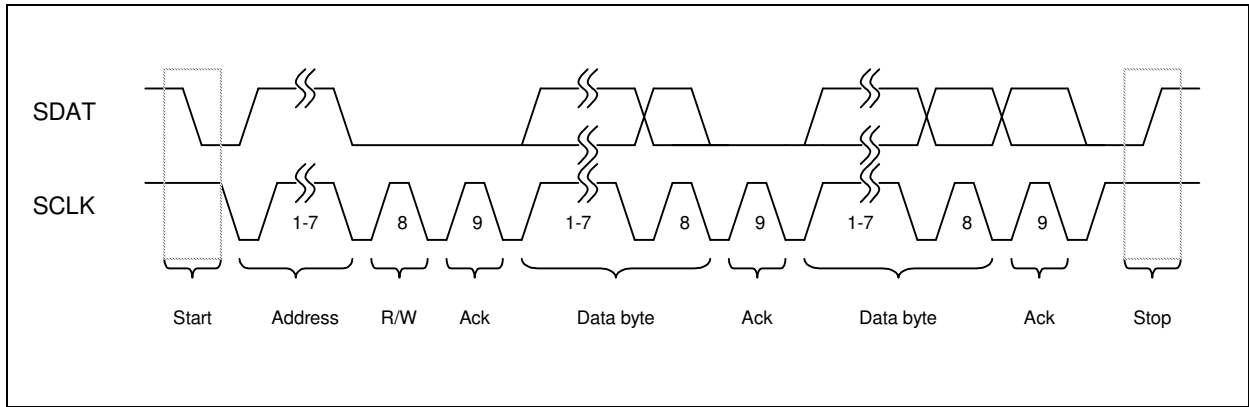


Figure 4: Data transfer principle of serial bus

1.3.2.3. MSI 01 Addressation Model

MSI 01 addressation is performed in two steps. Initially, a device must be selected. This is done by sending the respective device address (DevID). The DevID of the MSI 01 is 0010001. It should unequivocally identify the MSI 01 within the destination bus system. For this reason, it must not be identical with the DevID of another device. In a second step, the destination address of the register to be accessed needs to be sent (RegID). Only then the actual data follows. Based on this model, the following protocols are possible for reading from, or writing into, a register:

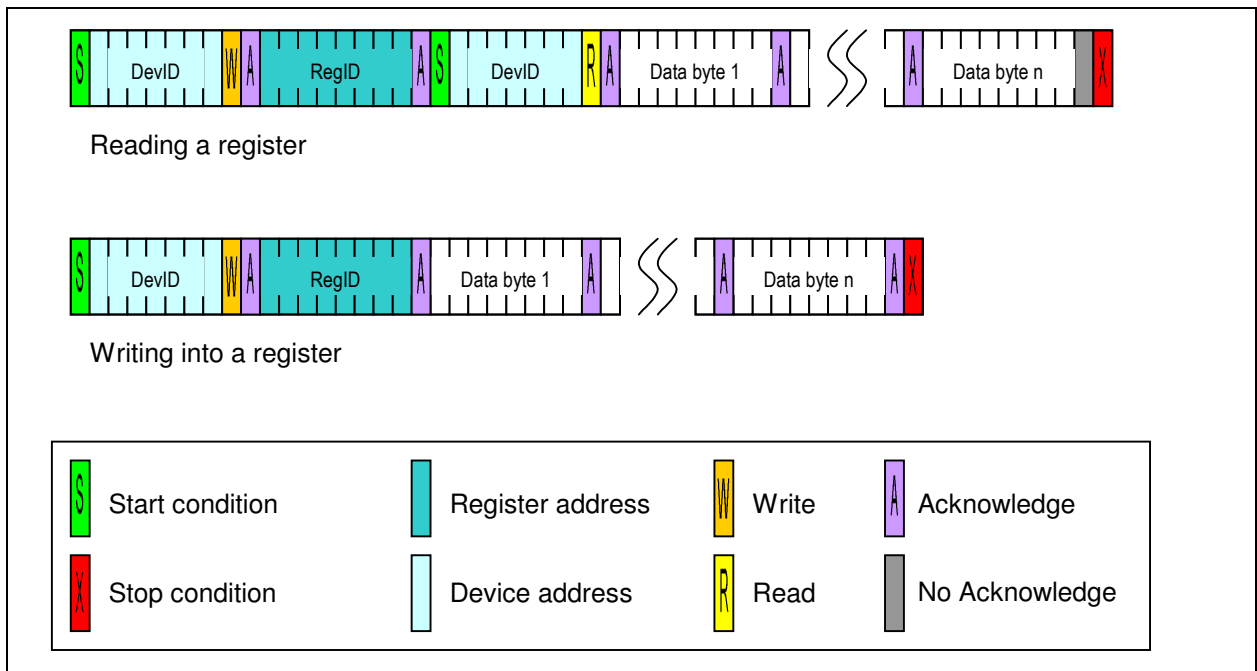


Figure 5: Register write and read operations

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

1.3.2.4. Overview of Permissible Application Commands

Only those commands which are quoted in the table below are supported by the serial interface. Other combinations are possible for testing purposes (register read/write operations), but are not guaranteed and supported in terms of functionality.

Addressed register	Read/Write	Effect
KONFIG	Read/Write	Cnfigures conversion parameters, starts a conversion if SW=1
ERGEB	Read	Reads conversion result
ERGSUM	Read	Reads sum value and OF bit
RTCSET	Read/Write	Reads RTC counter / sets RTC counter to its starting value and resets ERGSUM of counter
GRENZ	Read/Write	Reads limit values / writes limit values
IMPZAHL	Read	Reads pulse counter
ZEITZA	Read	Reads time counter
PORT	Read/Write	Reads / writes address
MODE	Read/Write	Reads / writes IC configuration
RTCVT	Read/Write	Reads / writes division factor

1.3.3. Logic Control Block

The implementation of a logic control block was necessary in order to facilitate a handshake procedure between the various MSI 01 components. It is responsible for sequencing control of the various measurements, providing a power-down functionality and synchronizing the MSI 01 components with each other.

Its control part creates the clock base for AD conversion. A conversion cycle may be triggered via the KONFIG bit SW (processor measurement) or via RTCSET and the RTC input in cyclic mode. A non-cyclic conversion begins after the module receives notice of a set SW bit. If a cyclic time-controlled conversion is triggered, the conversion process will start on arrival of a RTCINT pulse (predivided RTC pulse) and subject to the condition that RTCSET is unequal zero, that no other conversion is taking place at this moment and the limit value flag contains zero. During these so-called background measurements, the BUSY signal stays high until the last measurement has been completed (RTC counter is down to zero or limit value exceeded).

The clock base procedure itself (Figure 6) begins with the clock generator getting started and the power-down state being abolished. It continues by:

- turning the bridge supply voltage on,
- configuring the amplifier channel (span, zero, resolution),
- expiry of the bridge setup time pre-selected via ST,

VERSION		
NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

- connecting the channel to the predefined source,
- compensation of the preamplifier offset,
- turning the chopper on,
- and performing actual AD conversion on expiry of the signal settling time.

On completion of a conversion the result will be available in the result counter. If conversion was triggered by a RTCINT pulse, the ERGSUM counter will continue to count too. If an overflow occurs in a RTCINT-triggered conversion, the OF bit of the ERGSUM counter will be set. Following a conversion, all analog components are switched back to power-down mode. A result counter reset takes place with each start of an A/D conversion. The ERGSUM counter is reset on loading of the RTCSET register. BUSY in low state indicates either the end of a processor measurement or the end of a succession of background measurements and, hence, its readiness to read the corresponding result from the ERGEB or the ERGSUM counter. With the trailing edge of BUSY the SW bit of the configuration register will be set to zero. As long as the BUSY signal is high, access to the ERGEB or ERGSUM counter is disabled.

On supply of operating voltage (V_{BAT}) these registers are set to their default state ('0') and the circuit remains in power-down state. The supply voltage (V_{DDA}) then takes on its maximum value. As long as the PON signal is active, the MISI 01 output signals are undefined.

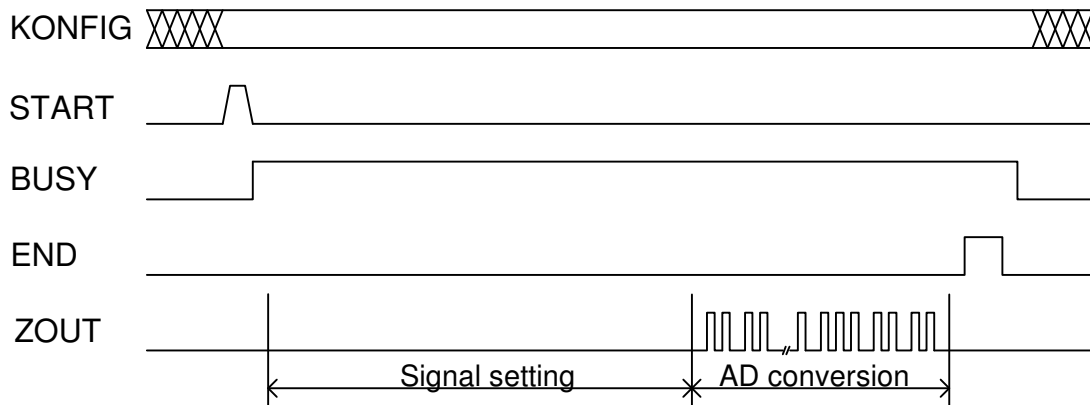


Figure 6: Clock diagram of analog part control signals

1.3.4. Signal Declarations

1.3.4.1. RTC Input

The RTC input has a Schmitt trigger input stage. Signals arriving at it are accepted with their '0'-'1'-transition edge. The RTCINT pulse is generated from the RTC pulse based on the relationship VT:1. If VT is '0', no RTCINT pulse will be generated.

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

1.3.4.2. Pulse Counter Input PULSE

The PULSE input has a Schmidt trigger input stage. Signals arriving at the input are counted with their '0'- '1' edge.

1.3.4.3. BUSY Output

The BUSY output is high-active. It is enabled on starting of a foreground measurement or the first in a series of background measurements. It is disabled on completion of a foreground measurement or the last in a series of background measurements.

1.3.4.4. Interrupt Output INT

The interrupt output provides interrupt pulses of approximately 4 μ s length depending on the logic state of the INT[1:0] and POL bits of the MODE register:

POL = 0 Low-active interrupt pulse

POL = 1 High-active interrupt pulse

INT[1:0] = 0 No interrupt pulses

INT[1:0] = 1 Interrupt on disablement of BUSY signal (internal END signal in clock diagram Figure 6)

INT[1:0] = 2 Interrupt on RTCINT if BUSY = low

INT[1:0] = 3 Interrupt pulses on END or RTCINT if BUSY = low

1.3.4.5. PON Output

This output delivers a high-active pulse when battery voltage is supplied (power on) or when the regulator output voltage drops to about 8% below nominal level (power fail). The output remains enabled for at least 100 μ s after reaching or restoring nominal regulator output voltage.

1.3.4.6. TEST Input

This input is low-active. Its purpose is to enable MSI 01 test mode. In a given application scenario, this input needs to be connected to high level or be left unused (internal pull up).

1.3.4.7. PU Input

This input is high-active. It can be used to cancel power-down state by bypassing the logic control block. In a given MSI 01 application, this input needs to be connected to low level or be left unused (internal pull down).

1.3.4.8. FCL Input

Can be used for external clock triggering of the MSI 01 with CMOS levels (about 250 kHz). In free-running mode, the FCL input pin must not be wired, because capacitive loads will decrease the frequency of the internal clock generator!

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

2. Electric Parameters

2.1. Absolute Limit Values

Parameter	Limits
Voltage at pin V_{BAT} to V_{SS}	7.2 V
Supply voltage V_{DD} to V_{SS}	5.5 V
Voltage at all other pins to V_{SS}	-0.3 V to $V_{DD} + 0.3$ V
Power dissipation at 70 °C	0.2 W
Operating temperature range	-20 °C to + 70 °C
Storage temperature range	-50 °C to +150°C
Lead temperature (soldering, 10sec.)	300 °C

2.2. Operating Parameters

Parameter	Min	Nom	Max	Unit
Battery voltage	3.7	6	6.6	V
Battery voltage source resistance			5	Ω
Ambient temperature	-20		70	°C
Low level input voltage at digital inputs			0.3	V
High level input voltage at digital inputs	0.9 V_{DD}			
Load current at pin VDD		12.5	30	mA
Capacitor at pin VBAT	t.b.d.	470	1000	nF
Capacitor at pin VDD	t.b.d.	10		μ F
Capacitor at pin VDDA	220			nF
Bridge resistance in voltage mode	2		5	k Ω
Bridge resistance in current mode	3		4	k Ω
Load capacitance at pin SDAT			100	pF
Clock frequency at pin SCLK			400	kHz
Rise/fall time at pin SCLK			1	μ s
Clock frequency at pin CLK	100	256	300	kHz
Rise/fall time at pin CLK			100	ns
Capacitor at pins AGND, SGND		t.b.d.	10	nF

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

2.3. AC/DC Features

($V_{BAT} = 3.7V \dots 7.2V$, $T_{AMB} = -20^{\circ}C \dots 70^{\circ}C$) ¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Management						
I_{BAT}	Supply current from battery	No bridges		2	3	mA
I_{BATPD}	Power down supply current	With bridges		3	5	μA
V_{DD}	Regulated supply voltage	Uncalibrated	3.0	3.3	3.6	V
V_{DD}	Regulated supply voltage	After calibration	3.2	3.3	3.4	V
TC_{VDD}	TC of supply voltage	$\Delta V_{DD}/(V_{DD} \Delta T_A)$	-400		400	ppm/K
VC_{VDD}	Line regulation	$\Delta V_{DD}/\Delta V_{BAT}$		7	15	mV/V
IC_{VDD}	Load regulation	$\Delta V_{DD}/\Delta I_{LOAD}$		5	10	mV/mA
V_{BAToff}	Power fail level	PD, $I_{LOAD} < 0.1mA$	0.91	0.923	0.94	V_{DD}
V_{BATon}	Power on level	$I_{LOAD} < 0.1mA$	0.95	0.96	0.97	V_{DD}
t_{RESET}	Reset pulse delay after power on or reset pulse width in case of power fail		100	200	500	μs

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

Bridge Current Sources 1, 2						
I_{OUT}	Source current, 8 steps	$V_{OUT} < V_{DD} - 0.4V, 2)$	0.041		0.060	V_{DDA}/R_{IB}
ΔI_{OUT}	Step width	2)		0,0027		V_{DDA}/R_{IB}
$TC_{I_{OUT}}$	Additional nonratiometric TC	$TC_{RIB} = 0, 2)$	-10		10	ppm/K
R_{SOURCE}	Source resistance	$V_{OUT} < V_{DD} - 0.4V$	10000	100000		R_{IB}
Ratiometric True Differential Analog Channels 0 ... 5, $V_{DD}=3.3V$, $R_{ADC} = 15Bit$						
V_{SPAN}	Voltage span, Span0	$V_{INMAX}-V_{INMIN}, 2)$		270		mV
V_{LSB}	Sensitivity, Span0	2)		8.63		$\mu V/cnt$
V_{SPAN}	Voltage span, Span1	$V_{INMAX}-V_{INMIN}, 2)$		90		mV
V_{LSB}	Sensitivity, Span1	2)		2.88		$\mu V/cnt$
V_{SPAN}	Voltage span, Span2	$V_{INMAX}-V_{INMIN}, 2)$		30		mV
V_{LSB}	Sensitivity, Span2	2)		0.96		$\mu V/cnt$
V_{SPAN}	Voltage span, Span3	$V_{INMAX}-V_{INMIN}, 2)$		10		mV
V_{LSB}	Sensitivity, Span3	2)		0.32		$\mu V/cnt$
V_{CM}	Common mode voltage		1.2		$V_{DD}-1.4$	V
Z_0	Zero count, Zero0	$V_{IN} = 0$	1950	2048	2150	counts
Z_0	Zero count, Zero1	$V_{IN} = 0$	3900	4096	4300	counts
Z_0	Zero count, Zero2	$V_{IN} = 0$	7800	8192	8600	counts
Z_0	Zero count, Zero3	$V_{IN} = 0$	15600	16384	17200	counts
$Z_{AZ} - Z_0$	Offset count	Span3	-3		3	counts
N_{PP}	Peak to peak output noise	Span3, 10 samp. AZ		4	6	cnt
N_{PP}	Peak to peak output noise	Span2, 10 samp. AZ		1	2	cnt
INL	Integral nonlinearity	Dev. from best strait	-300		300	ppm
TC_{GAIN}	Temp. dependency of gain		-25		25	ppm/K

Analog Channel 6, Internally Connected to TEMPSENS, $V_{DD}=3.3V$, $R_{ADC}=13 Bit$						
V_{MAX}	Full bat count	$V_{BAT} = 6.6V, Zero3, 2)$		2579		counts
V_{MIN}	Low bat count	$V_{BAT} = 3.6V, Zero3, 2)$		1200		counts
V_{LSB}	Sensitivity	2)		2.17		mV/cnt
Z_{AZ}	Auto zero count	Zero3	3900	4096	4300	counts
INL	Integral nonlinearity	Dev. from best strait	-1000		1000	ppm
Analog Channel 7, Internally Connected to V_{BAT} , $V_{DD}=3.3V$, $R_{ADC}=13 Bit$						
Z_{25}	Output count at 25°C	Zero3	5000		6000	counts
V_{LSB}	Sensitivity	2)	0.15	0.2	0.25	K/cnt
Z_{AZ}	Auto Zero count	Zero3	3900	4096	4300	counts
INL	Integral nonlinearity	Dev. from best strait	-500		500	ppm

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

Digital Inputs / Outputs						
I_{IH}	Input current	Pin CLK			15	μA
I_{IL}	Input current	Pin CLK	-15			μA
V_{OH}	Output high level	$I_o = 2mA$	$V_{DD}-0.3$			V
V_{OL}	Output low level	$I_o = -2mA$			0.3	V
t_P	Pulse length at INT	high	2		10	us
Clock Generator						
f'_{CLK}	Clock frequency	Free running, $C_{CLK} = 0$	200	256	300	kHz
A to D Converter						
R_{ADC}	Resolution		9		15	Bit
t_{CONV}	Conversion time	$f_{CLK}=256kHz, 15Bit$			128	ms
t_{CONV}	Conversion time	$f_{CLK}=256kHz, 9Bit$			2	ms
DNL	Differential nonlinearity	no missing codes			0.9	LSB
Total System, $R_{ADC}=15Bit, Zer0, Span3, Tamb = -20 \dots 40^{\circ}C$						
E_{VMODE}	Overall error	V-mode, average over 10 samples			56	counts
E_{IMODE}	Overall error	I-mode, average over 10 samples			68	counts

For reliability reasons, the maximum battery voltage of 7.2V is not allowed for permanent operation.

- 1) Parameter is ratiometric (i.e. its nominal value must be multiplied with $V_{DDA} / 3.3V$)

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

3. Description of MSI 01 Package

3.1. Ordering Specifications

Type designation	Supply version
MSI 01DF	DICE (unpackaged)
MSI 01GF	PQFP44
MSI-EB1	Evaluation Board with demo software, power pack, zero-modem cable

3.2. PQFP44 Package Dimensions

Phys. dimensions (based on JEDEC: MS-112AA)

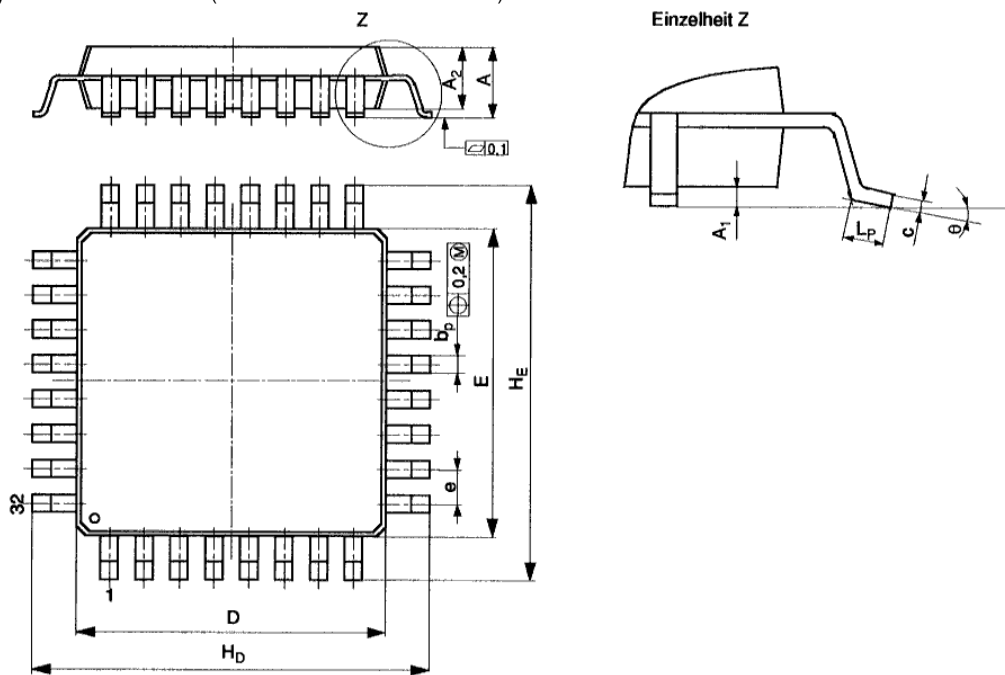


Figure 7: View of PQFP44 package

Dimensions of subgroup B1	
e_{norm}	0.80
A_{max}	2.60
b_{Pmin}	0.25
b_{Pmax}	0.45
H_{Emin}	13.65
H_{Emax}	14.30
H_{Dmin}	13.65
H_{Dmax}	14.30
L_{Pmin}	0.63

Dimensions of subgroup C1	
A_{min}	2.10
A_{1min}	0.15
A_{1max}	0.30
A_{2min}	1.80
A_{2max}	2.20
c_{min}	0.11
c_{max}	0.23
D_{min}	9.90
D_{max}	10.10
E_{min}	9.90
E_{max}	10.10
θ_{min}	0°
θ_{max}	10°

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

3.3. Pin-Out Assignments

No.	Name	Description	ESD protection	PQFP 44 pin	ground
1.	VBAT	Battery voltage	2kV	16	VSSA
2.	VDDA	Controlled supply voltage for MSI 01	2kV	17	VSSA
3.	VDD	Controlled supply voltage for controller	2kV	18	VSS
4.	VSS	Digital VSS	2kV	38	
5.	VSSA	Analog VSS	2kV	39	
6.	n.c.			15	
7.	SGND	Analog ground, SC circuitry parts (VDD/2)	2kV	40	VSSA
8.	VBN	Negative bridge supply voltage	1.2kV	41	VSSA
9.	VBP	Positive bridge supply voltage	1.2kV	6	VSSA
10.	VBP0	Positive supply of calibration divider	1.2kV	44	VSSA
11.	VBP1	Positive bridge supply, bridge 1	1.2kV	4	VSSA
12.	VBP2	Positive bridge supply, bridge 2	1.2kV	8	VSSA
13.	VBP3	Positive bridge supply, bridge 3	1.2kV	12	VSSA
14.	RIB1	Low TC resistor for current source 1	1.2kV	5	VSSA
15.	RIB2	Low TC resistor for current source 2	1.2kV	7	VSSA
16.	IP0	Positive input 0	1.2kV	43	VSSA
17.	IN0	Negative input 0	1.2kV	42	VSSA
18.	IP1	Positive input of bridge 1	1.2kV	3	VSSA
19.	IN1	Negative input of bridge 1	1.2kV	2	VSSA
20.	IC1	Input of divider 1	1.2kV	1	VSSA
21.	IP2	Positive input of bridge 2	1.2kV	9	VSSA
22.	IN2	Negative input of bridge 2	1.2kV	10	VSSA
23.	IC2	Input of divider 2	1.2kV	11	VSSA
24.	IP3	Positive input of bridge 3	1.2kV	13	VSSA
25.	IN3	Negative input of bridge 3	1.2kV	14	VSSA
26.	FCL	Clock frequency C or clock input	2kV	37	VSSA
27.	SCLK	Clock input of interface	2kV	33	VSS
28.	SDAT	Data input/output of interface, open drain	2kV	32	VSS
29.	PON	Power on, power fail output	2kV	19	VSS
30.	RTC	Real time clock	2kV	21	VSS
31.	INT	Interrupt output	2kV	20	VSS
32.	BUSY	BUSY output	2kV	36	VSS
33.	PU	Power up input (default = low)	2kV	35	VSS
34.	PULSE	Pulse counter input	2kV	22	VSS
35.	PB0	PortBit 7	2kV	23	VSS
36.	PB1	PortBit 6	2kV	24	VSS
37.	PB2	PortBit 5	2kV	25	VSS
38.	PB3	PortBit 4	2kV	26	VSS
39.	PB4	PortBit 3	2kV	27	VSS
40.	PB5	PortBit 2	2kV	28	VSS
41.	PB6	PortBit 1	2kV	29	VSS
42.	PB7	PortBit 0	2kV	30	VSS
43.	TEST	Turns digital test mode on (default = high)	2kV	34	VSS
44.	n.c.		2kV	31	

NO.	ISSUE	APPROVED
1	V 1.4	2002-07-09

4. Application Circuit

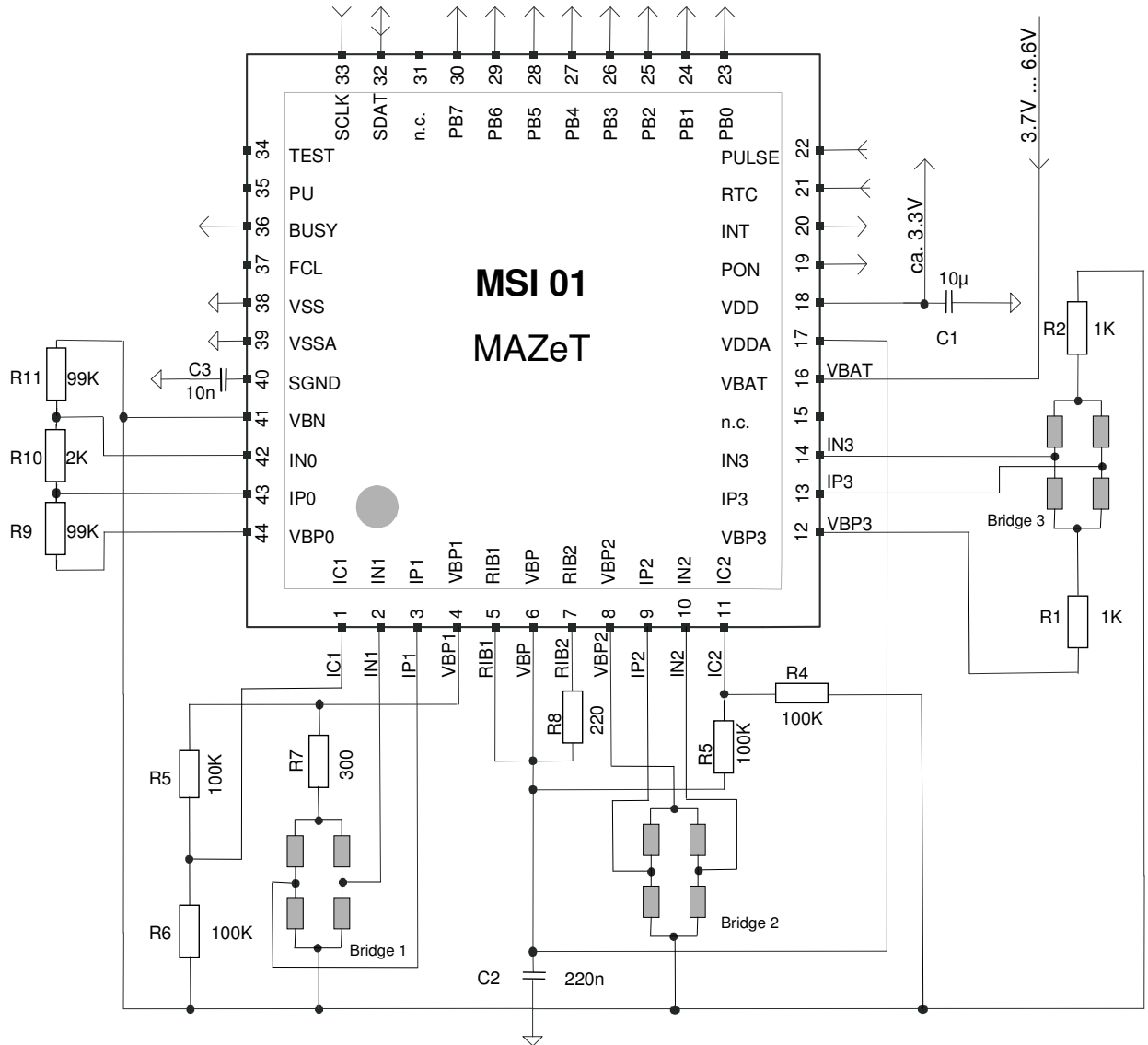


Figure 8: Application wiring diagram of MSI 01

For more information, please contact:

MAZeT GmbH
Sales office:
Dr. Winfried Mahler
 Göschwitzer Straße 32
 07745 JENA
 GERMANY
 Phone: +49 3641 2809-0
 Fax: +49 3641 2809-12
 E-Mail: mahler@MAZeT.de
 Url: <http://www.MAZeT.de>